Session 10 Overview

mm-Wave Tranceivers and Building Blocks

Chair: Ali Niknejad, *University of California, Berkeley, CA*

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Technology scaling and Moore's law have paved the way for ever faster transistors, with device unity gain frequency (f_t) exceeding 100GHz for today's 90nm CMOS technology. The realization of functional circuits operating at or above the device f_t is a challenging task, and the subject of much of this session, with demonstrations of circuits operating above the f_t and close to the device f_{max}. The main advantages of Si-based technologies are the promise of high levels of integration and low manufacturing cost. In fact, in this session we see several highly integrated CMOS and SiGe front-end receivers and frequency synthesizers integrated into a single chip operating in the mm-wave frequency range.

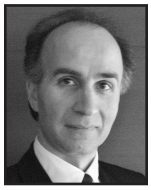
Operation of high frequencies has several interesting and important applications. The 60GHz band offers a wide unlicensed spectrum allowing extremely high data rate multi-Gb/s communication systems. Traditionally 60GHz radios were built as modules with expensive III-V technologies. The realization of low-cost integrated circuit solutions will allow widespread commercial deployment of multi-Gb/s communication devices, allowing short range personal area networks for downloading multimedia (video) to mobile devices, Gb/s wireless LAN for an untethered connection to the network, and high data rate point-to-point communication and indoor video transmission. The key technology challenges to compete in this market are low-noise operation, high output power capability, and low phase-noise voltage-controlled oscillators.

Moving beyond 60GHz opens the door to new potential applications such as automotive radar, medical imaging, and security. Due to the high cost of mm-wave electronics, today only high-end automobiles are equipped with radar for automatic cruise control and safety. Implementation of such systems in Si integrated circuits can reduce the cost by an order of magnitude, enabling ubiquitous adoption of radar, increasing the safety and security of transportation. Other potential applications include mm-wave medical imaging as a low-cost non-ionizing alternative to x-rays.

The session begins with the three of the first reported highly integrated CMOS mm-wave transceivers. Paper 10.1 from UCLA demonstrates a 50GHz CMOS heterodyne receiver in 90nm technology. The chip includes the LNA, mixer, LO and divider. Paper 10.2 from UC Berkeley and SiBEAM presents a 60GHz highly integrated receiver in 0.13µm technology, including the LNA, mixer, LO, and frequency doubler. Paper 10.3 from National Taiwan U describes a fully integrated 60GHz 0.13µm CMOS six-port transceiver which includes transmit and receive amplifiers, RF switch, transmit VCO and modulator, and a six-port power detector. This paper demonstrates successful demodulation of data up to 4Gb/s using BPSK modulation. All three papers represent the state-of-the-art in integration of CMOS mm-wave circuits into a single chip.

Paper 10.4 from TU Delft and IBM presents a varacterless VCO in 0.13µm CMOS that operates from 23 to 29GHz using a coupled-inductor tuning scheme. In Paper 10.5 by National Taiwan U, the first 60GHz synthesizer realized in 90nm CMOS technology is presented with record levels of integration and phase noise for CMOS mm-wave applications. Paper 10.6 from Bochum Rohr-U describes a divider with record speed performance as fast as 90GHz that is realized with an injection-locked topology in a 65nm CMOS process.

Paper 10.7 from UC Berkeley includes the world's fastest CMOS tuned amplifier, working up to 104GHz in a 90nm CMOS process. This paper also demonstrates record power performance for a 60GHz amplifier, and a high output power 104GHz oscillator. The final paper of the session, Paper 10.8 by Caltech, describes a highly integrated bidirectional SiGe phase shifter for RF-combining phased-array applications.



10.1 A mm-Wave CMOS Heterodyne Receiver with On-Chip LO and Divider **8:30 AM**

B. Razavi, University of California, Los Angeles, CA

A heterodyne RX incorporates an LNA, RF and I/Q IF mixers, nested inductors, and a passive-mixer-based Miller divider. Fabricated in a 90nm CMOS process, the RX achieves an NF of 6.9 to 8.3dB from 49 to 53GHz with a gain of 26 to 31.5dB and an I/Q mismatch of 1.6dB/6.5°. The circuit consumes 80mW from a 1.8V supply.

10.2 A Highly Integrated 60GHz CMOS Front-End Receiver **9:00 AM**

S. Emami, University of California, Berkeley, CA

A 60GHz CMOS front-end receiver is described. The receiver comprises an LNA, a quadrature-balanced downconversion mixer, a VCO, and a frequency doubler. The integrated front-end has a conversion gain of 11.8dB, an NF of 10.4dB, and an input P_{1dB} of -15.8dBm. The receiver is implemented in a digital 0.13µm CMOS process and draws 64mA from a 1.2V supply.

10.3 A 60GHz Low-Power Six-Port Transceiver for Gigabit Software-Defined Transceiver Applications **9:30 AM**

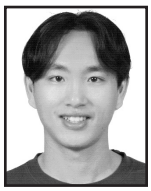
C-H. Wang, National Taiwan University, Taipei, Taiwan

A 60GHz six-port transceiver IC in a standard-bulk 0.13µm CMOS process is reported. This chip is composed of a VCO, a modified reflection-type I/Q modulator, a buffer amplifier, an SPDT switch, an LNA, and a six-port detector. The measured results show 4.5dB conversion gain and 4Gb/s modulation BW with 97.7mW DC power consumption.

10.4 A 23-to-29GHz Differentially Tuned Varactorless VCO in 0.13µm CMOS **10:15 AM**

K. Kwok, Delft University of Technology, Delft, The Netherlands

A differentially tuned varactorless VCO is implemented in a 0.13µm CMOS process. The frequency is continuously tunable from 23.2 to 29.4GHz (23.6% range differential and 3.3% range for common-mode tuning) using a single-ended (1.5V max) tuning voltage. Measured phase noise at 26.6GHz is -96.2dBc/Hz (3MHz offset) and the open-drain output buffer delivers -11dBm (single-ended) to a 50Ω load. The 0.3×0.4mm^2 core consumes 43mW (6.5mW in the output buffer) from a 1.2V supply.



10.5 A 58-to-60.4GHz Frequency Synthesizer in 90nm CMOS **10:30 AM**

C. Lee, National Taiwan University, Taipei, Taiwan

A 58-60.4GHz frequency synthesizer is implemented in a 90nm CMOS process. A VCO with a distributed-LC tank and a current-reuse frequency divider are used. For 60.4GHz, the measured phase noise at 1MHz and 2MHz offset is -85.1dBc/Hz and -95dBc/Hz, respectively. Including the buffers, the chip consumes 80mW from a 1.2V supply.

10.6 A 90GHz 65nm CMOS Injection-Locked Frequency Divider **11:00 AM**

P. Mayr, Ruhr-Universität Bochum, Bochum, Germany

Two injection-locked 2:1 frequency dividers for automotive radar applications achieve locking ranges from 82 to 94.1GHz and from 34.3 to 42.1GHz and consume 4mW and 8.4mW, respectively. The cascade of the two dividers can be locked from 79.7 to 81.6GHz. The 1mm^2 chip is implemented in a 65nm CMOS process.

10.7 Low-Power mm-Wave Components up to 104GHz in 90nm CMOS **11:15 AM**

B. Heydari, University of California, Berkeley, CA

A customized 90nm device layout yields an extrapolated f_{max} of 300GHz. The device is incorporated into a low-power 60GHz amplifier consuming 10.5mW, providing 12dB of gain, and an output P_{1dB} of 4dBm. An experimental 3-stage 104GHz amplifier has a measured peak gain of 9.3dB. Finally, a Colpitts oscillator at 104GHz delivers up to -5dBm of output power while consuming 6mW.

10.8 A Bidirectional RF-Combining 60GHz Phased-Array Front-End **11:45 AM**

A. Natarajan, California Institute of Technology, Pasadena, CA

A 60GHz RF-combining phased-array front-end is implemented in silicon using a hybrid parallel/series phase-shift approach that reduces the requirements of the on-chip phase shifters. The 4-element array provides for simultaneous illumination of 2 angles of incidence and includes amplitude control and continuous phase adjustment. The front-end NF <6.9dB at 60GHz and the array achieves full spatial coverage with peak-to-null ratio >25dB. It consumes 265mW and occupies 4.6mm^2.